INFORMAZIONI PERSONALI

Massimo Poncino

Sesso | Data di nascita | Nazionalità

POSIZIONE RICOPERTA Professore Ordinario di Sistemi di Elaborazione dell'Informazione, Politecnico di Torino, Torino.

ESPERIENZA PROFESSIONALE

Da 10/2006	Professore Ordinario di Sistemi di Elaborazione dell'Informazione presso il Dipartimento di Automatica e Informatica del Politecnico di Torino, Torino
Da 10/2004 a 10/2006	Professore Associato di Sistemi di Elaborazione dell'Informazione presso il Dipartimento di Automatica e Informatica del Politecnico di Torino, Torino
Da 10/2001 a 10/2004	Professore Associato di Sistemi di Elaborazione dell'Informazione presso il Dipartimento di Informatica dell'Università di Verona, Verona
Da 7/1995 a 10/2001	Ricercatore di Sistemi di Elaborazione dell'Informazione presso il Dipartimento di Automatica e Informatica del Politecnico di Torino, Torino
Da 4/1994 a 7/1995	Borsa di Ricerca post-dottorato presso il Dipartimento di Automatica e Informatica del Politecnico di Torino, Torino
Da 3/1993 a 4/1994	Visiting Researcher presso il Dipartimento di Electrical and Computer Engineering della University of Colorado, Boulder, USA.
Da 1/1990 a 1/1993	Dottorato di Ricerca in Ingegneria Informatica e dei Sistemi presso il Dipartimento di Automatica e Informatica del Politecnico di Torino, Torino

ISTRUZIONE E FORMAZIONE

Ottobre 1993	Dottorato di Ricerca in Ingegneria Informatica e dei Sistemi, Politecnico di Torino, Torino
Luglio 1989	Laurea in Ingegneria Elettronica, Politecnico di Torino con votazione 107/110.

COMPETENZE PERSONALI

Lingua madre: Italiano

Altre lingue

	COMPRENSIONE		PARLATO		PRODUZIONE SCRITTA
	Ascolto	Lettura	Interazione	Produzione orale	
Inglese	Ottimo (C2)	Ottimo (C2)	Ottimo (C2)	Ottimo (C2)	Ottimo (C2)
Spagnolo	Base (A1)	Base (A1)	Base (A1)	Base (A1)	-

Competenze organizzative e gestionali
- Esperienza di gestione gruppi di lavoro e risorse umane
- Esperienza di preparazione, gestione tecnica e finanziaria di progetti di ricerca finanziati
- Gestione ed organizzazione di convegni scientifici (v. allegato)

Competenze professionali
- Esperienza su sistemi di elaborazione digitali in generale con particolare enfasi su aspetti legati al consumo energetico dei dispositivi.

Patente di guida: B

ULTERIORI INFORMAZIONI

Pubblicazioni

Autore di circa 300 pubblicazioni scientifiche tra libri, capitoli di libro, articoli su riviste internazionali e articoli in atti di conferenze internazionali. L'elenco complessivo è disponibile online su (*http://porto.polito.it/view/creators/Poncino=3AMassimo=3A002156=3A.html*)

Presentazioni, Conferenze, Seminari

Autore di oltre 100 presentazioni tecnico-scientifiche a conferenze internazionali (di cui 11 "tutorial") e seminari presso aziende e Università internazionali (in Europa, Asia e Stati Uniti).

Progetti

Responsabile tecnico/scientifico dei seguenti progetti di ricerca finanziati

- ESPRIT-OMI 20.761 "ASCISSA" (Adopting SCI and SSA Interconnects in advanced microprocessor-based PC Servers), 1994-1996.
- ESPRIT 26.796 "PEOPLE" (Power Estimation for Fast Exploration of Embedded Systems), 1997-2000.
- IST-2000-30093 "EASY" (Energy-Aware SYstem-on-chip design of the HIPERLAN/2 standard), 2001-2004.
- IST-2001-11476 "POET" (Power Optimizations for Embedded sysTems), 2001-2004.
- IST-2001-34607 "SYMBAD" (Formal Verification in System Level Based Design), 2002-2005.
- IST-4-026980 "CLEAN" (Controlling Leakage Power in NanoCMOS SoCs), 2005-2008.
- CRAFT "MAP^{2}" (Micro-Architectural Power Management: Methods, Algorithms and Prototype Tools), 2006-2008.
- JU ENIAC "MODERN" (Modeling and Design of Reliable, process variation-aware Nanoelectronic devices, circuits and systems), 2009-2012.
- FIRB "DAMASCO" (Data Acquisition and MAnagement in a Sensing and COmmunicating environment), 2006-2011. Prof. Poncino was the coordinator of this .
- JU ARTEMIS "SMECY" (Smart Multicore Embedded Systems), 2010-2012
- IST-7-24799 "COMPLEX" (COdesign and power Management in PLatform-based design space EXploration), 2010-2013.
- JU ENIAC, "ERG" (Energy for a Green Society: From Sustainable Harvesting to Smart Distribution. Equipments, Materials, Design Solutions and Their Applications), 2011-2014-
- JU ENIAC "MOTORBRAIN" (Nanoelectronics for Electric Vehicles Intelligent Failsafe PowerTrain), 2011-
- IST-7-288827 "SMAC" (SMArt systems Codesign), 2011-2015
- JU ENIAC "IDEAS" (Interactive Power Devices for Efficiency in Automotive with Increased Reliability and Safety), 2012-2015
- IST-7-611146 "CONTREX" (Design of embedded mixed-criticality CONTRol systems under consideration of EXtrafunctional properties), 2013-2016

Riconoscimenti e Premi

- Recognition of Service Award (2013) - ACM (Association for Computing Machinery)
- Senior Member IEEE (Institute of Electronic and Electrical Engineers) - 2012
- Certificare of Appreciation - IEEE Circuits and Systems Society - 2004,2005,2006,2007,2008
- "Best Paper Award" (Miglior articolo) alla conferenza EuroDAC'96: IEEE European Design Automation Conference.
- "Best Paper Award" (Miglior articolo) alla conferenza GLS-VLSI-08: ACM/IEEE 18th Great Lakes Symposium on VLSI

Appartenenza a gruppi / associazioni

- Senior Member IEEE (Institute of Electronic and Electrical Engineers) - 2012
- Membro of the Council of Communications Advisors.
- Membro of the Circuit and Systems Society.
- Membro del Comitato Esecutivo della conferenza *International Symposium on Low-Power Electronics and Design*

Dati personali

Autorizzo il trattamento dei miei dati personali ai sensi del Decreto Legislativo 30 giugno 2003, n. 196 "Codice in materia di protezione dei dati personali".

ALLEGATI

Si allega elenco dettagliato di competenze, esperienze e pubblicazioni.

1. Attività Scientifica e Professionale

Professional Experiences

- Senior Member of the IEEE.
- Valutatore di progetti IST (Information Society Technologies) Per la Commissione Europea nel contesto del VI Programma Quadro (2003), area "Embedded Systems".
- Valutatore di progetti IST (Information Society Technologies) Per la Commissione Europea nel contesto del VII Programma Quadro (2011-2013), area "Very Advanced Nanoelectronic Components'" and "Smart Systems"
- Valutatore di proposte di ricerca per la Research Promotion Foundation (RPF) di Cipro (2011).
- Valutatore di proposte di ricerca e innovazione per la Swiss National Science Foundation (2011).
- Valutatore di proposte di ricerca per il Ministero dell'Istruzione e della Scienza della Federazione Russa (2013).
- Valutatore di proposte di ricerca e innovazione per il Ministero dell'Istruzione e della Scienza del Kazakhstan (2014).
- Valutatore di proposte di ricerca per il Ministero dell'Istruzione e della Ricerca (MIUR) (2006-).
- Membro del Council of Communications Advisors.
- Membro del Circuit and Systems Society.

Partecipazioni a Comitati Editoriali di Riviste

- Associate Editor, IEEE Design & Test (2013-)
- Associate Editor, ACM Transactions on Design Automation of Embedded Systems (2012-)
- Associate Editor, International Journal of Electrical Electronics and Telecommunications (2012-).
- Associate Editor, International Journal of Engineering Research and Science & Technology (2012-)
- Associate Editor, Consumer Electronics Times (2012-).
- Associate Editor, Journal of Electrical and Computer Engineering (2010-)
- Associate Editor, Research Letters in Electronics (2009)
- Associate Editor, International Journal of Design, Analysis and Tools for Integrated Circuits and Systems (2009-)
- Associate Editor, EABM - Recent Patents on Electrical Engineering (2007-)
- Associate Editor, IEEE Transactions on Computer-Aided Design (2006-2011)
- Associate Editor, Indo-American Journal of Electrical Electronics Engineering (2013-).
- Guest Editor, International Journal of Design, Analysis and Tools for Integrated Circuits and System- June 2011.
- Guest Editor, EURASIP Journal on Embedded Systems (Special Issue su "Design Techniques and Algorithms for Power Modeling, Estimation, and Optimization in Embedded Systems") - Spring 2012.

Gestione di eventi internazionali

- Program Co-Chair dell *ACM/IEEE International Symposium on Low-Power Electronics and Design* – 2011.
- General Co-Chair del *ACM/IEEE International Symposium on Low-Power Electronics and Design* – 2012. ((>200 partecipanti, budget circa 100.000$)
- Publicity Chair del *IEEE International Conference of Computer Design* – 2014.

Partcipazione a comitati tecnici di conferenze internazionali

- *Design Automation Conference (DAC) – (2012-)*
- *International Conference on CAD (ICCAD) – (2011-)*
- *Design Automation and Test in Europe (DATE) – (2004-)*
- *IEEE Computer Society Annual Symposium on VLSI (2014)*
- *ACM International Symposium on Low-Power Electronics and Design (ISLPED) – (2000-)*
- *ASP-DAC: Asia/South-Pacific Design Automation Conference (2010-2011)*
- *IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS) - (2012-)*
- *ACM/IEEE Great Lakes Symposium on VLSI (GLS-VLSI) – (2006—)*
- *IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (2012-2013)*
- *International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS) – (2004-)*
- *IEEE Alessandro Volta Memorial Workshop on Low Power Design – 1999.*

- *European Workshop on CMOS Variability (VARI) – (2010-)*
- *International Conference on Design & Architectures for Signal & Image Processing (DASIP) – (2011, 2012)*
- *IEEE 10th International New Circuits and Systems Conference (NEWCAS) - 2012*
- *International Conference on Embedded Systems and Applications (ESA) – 2003.*
- *EDAA Ph.D. Forum 2003-2004.*
- *International Conference on Embedded Software and Systems (ICESS) – 2005-2008.*
- *IFIP International Conference on Very Large Scale Integration (VLSI-SoC) – 2008*
- *International Workshop on Web and Pervasive Security (WPS2008) – 2008.*
- *Int. Workshop on Trustworthiness, Reliability and services in Ubiquitous and Sensor networks (TRUST) – 2006-.*
- *Int Workshop on Application and Security service in Web and pervAsive eNvironments (ASWAN '07) – 2007.*
- *International Conference on Computational Science 2007 (ICCS 2007) -2007*
- *IFIP International Conference on Embedded And Ubiquitous Computing (EUC) – (2005, 2006, 2014)*
- *ICESS: International Conference on Embedded Software and Systems (2005,2008)*
- *International Conference on Computational & Experimental Engineering and Sciences (ICCES) - 2010*
- *WPS: International Workshop on Web and Pervasive Security (2008)*
- *SPPC: International Conference on Information Security and Assurance (2008)*
- *FCST: International Conference on the Frontier of Computer Science and Technology (2009)*
- *IEEE International Conference on Electronics, Circuits and Systems (ICECS) - (2010)*
- *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) - (2009,2010)*
- *International Conference on ICT as Key Technology against Global Warming - ICT-GLOW - (2011, 2012)*
- *International Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (PARMA) – (2009,2011-2013)*
- *International Conference on Architecture of Computing Systems (ARCS) – 2011, 2012*

Revisore per Riviste Internazionali

- *IEEE Transactions on Computers*
- *IEEE Transactions on Computer-Aided Design*
- *IEEE Transactions on VLSI Systems*
- *ACM Transactions on Design Automation of Electronic Systems*
- *ACM Journal of Emerging Technologies in Computing*
- *IEEE Transactions on Systems, Man and Cybernetics*
- *IEEE Transactions on Circuits and Systems I*
- *IEEE Transactions on Circuits and Systems II*
- *IEE Proceedings – Computers and Digital Techniques*
- *IEE Electronic Letters*
- *Integration: the VLSI Journal*
- *International Journal of Parallel Programming*

Riconoscimenti e Premi:

- Best Paper Award at *IEEE EuroDAC'96: IEEE European Design Automation Conference.*
- Best Paper Award at *GLS-VLSI-08: ACM/IEEE 18th Great Lakes Symposium on VLSI*
- Certificate of Appreciation by IEEE Circuits and Systems Society in recognition of the service as Associate Editor of the IEEE Transactions on CAD (2004-2005, 2006-2007, 2008)
- Recognition of Service Award by CEDA for serving as Technical Program Co-Chair of the 2011 International Symposium on Low-Power Electronics and Design
- Recognition of Service Award by ACM for serving as General Co-Chair of the 2012 International Symposium on Low-Power Electronics and Design

Tutorial o corsi tenuti nel contesto di conferenze internazionali

- "Design of Low-Power Circuits and Systems", Conference Tutorial at *IEEE EuroDAC,* 1995.
- "Programmable Devices: The Solution to Rapid System Design", Conference Tutorial at *IEEE 6th GLS-VLSI,* 1996.

- "High-Level Power Optimization of Digital CMOS Circuits and Systems," Conference Tutorial at *IEEE ISCAS*, 1999.
- "RTL And Gate-Level Power Optimization of Digital Circuits" Conference Tutorial at *IEEE ISCAS*, 2000.
- "RTL Power Optimization: Concepts, Tools, and Design Experiences," Conference Tutorial at IEEE *DATE*, 2004.
- "Coherent or not Coherent? What Programming Model for Energy-Efficient MPSoCs?" invited talk in the Power-Aware Computing Workshop, 2005.
- "Managing Leakage Power in Deep-Submicron Designs", Conference Tutorial at *IEEE ICECS'06*, 2006.
- "Managing Leakage Power in deep Submicron Designs ", *13th IEEE International Conference on Electronics, Circuits and Systems* (ICECS'07), 2006.
- "Post-Silicon Thermal-Aware Clock Distribution Network Design", invited seminar in the Power-Aware Computing Workshop,, 2007.
- "CAD Solutions for System-Level Power Optimization" *41st Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-41), 2008.*
- "Low Power: The power of Power in future wireless smart systems for the Internet of Things", Conference Tutorial at IEEE *DATE*, 2015.

2. Attivita' di Ricerca

L'attività scientifica di ricerca applicata di Massimo Poncino si focalizza sulla progettazione di sistemi digitali con particolare enfasi sull'ottimizzazione del consumo energetico di tali sistemi. Su questi argomenti (ed altri) ha pubblicato 1 libro, 6 capitoli di libro, oltre 70 articoli su riviste internazionali e oltre 200 in atti di conferenze internazionali (vedi allegato finale).

Gestione di progetti finanziati

Gli argomenti di ricerca hanno trovato notevole applicazione in un contesto di ricerca applicata industriale, come testimoniato dai progetti del quale Massimo Poncino ha svolto il ruolo di responsabile tecnico/scientifico.

- Project ESPRIT-OMI 20.761 "ASCISSA" (Adopting SCI and SSA Interconnects in advanced microprocessor-based PC Servers), 1994-1996.
- Project ESPRIT 26.796 "PEOPLE" (Power Estimation for Fast Exploration of Embedded Systems), 1997-2000.
- Project IST-2000-30093 "EASY" (Energy-Aware SYstem-on-chip design of the HIPERLAN/2 standard), 2001-2004.
- Project IST-2001-11476 "POET" (Power Optimizations for Embedded sysTems), 2001-2004.
- Project IST-2001-34607 "SYMBAD" (Formal Verification in System Level Based Design), 2002-2005.
- Project IST-4-026980 "CLEAN" (Controlling Leakage Power in NanoCMOS SoCs), 2005-2008.
- Project CRAFT "MAP²" (Micro-Architectural Power Management: Methods, Algorithms and Prototype Tools), 2006-2008.
- Project JU ENIAC "MODERN" (Modeling and Design of Reliable, process variation-aware Nanoelectronic devices, circuits and systems), 2009-2012.
- Project FIRB "DAMASCO" (Data Acquisition and MAnagement in a Sensing and COmmunicating environment), 2006-2011. Prof. Poncino was the coordinator of this project.
- Project JU ARTEMIS "SMECY" (Smart Multicore Embedded Systems), 2010-2012
- Project IST-7-24799 "COMPLEX" (COdesign and power Management in PLatform-based design space EXploration), 2010-2013.
- Project JU ENIAC, "ERG" (Energy for a Green Society: From Sustainable Harvesting to Smart Distribution. Equipments, Materials, Design Solutions and Their Applications), 2011-
- Project JU ENIAC "MOTORBRAIN" (Nanoelectronics for Electric Vehicles Intelligent Failsafe PowerTrain), 2011-
- Project IST-7-288827 "SMAC" (SMArt systems Codesign), 2011-2015
- Project JU ENIAC "IDEAS" (Interactive Power Devices for Efficiency in Automotive with Increased Reliability and Safety), 2012-2015
- Project IST-7-611146 "CONTREX" (Design of embedded mixed-criticality CONTRol systems under consideration of EXtrafunctional properties), 2013-2016

Lista di pubblicazioni

Libri

1. A. Macii, L. Benini, *M. Poncino*,
   Memory Design Techniques for Low-Energy Embedded Systems, Kluwer Academic Publishers, 2002.

Capitoli di Libro

1. "Micro-Architectural Power Estimation and Optimization,"
   E. Macii, R. Mehra, M. Poncino,
   in *Handbook of EDA for IC Design*,

G. Martin, L. Lavagno, and L. Scheffer Editors,
CRC Press, Boca Raton, Florida, 2005.

2. "System-Level Dynamic Power Management,"
N. Chang, E. Macii, M. Poncino, V. Tiwari,
in *Handbook of EDA for IC Design*,
CRC Press, Boca Raton, Florida, 2005.
3. E. Macii, M. Poncino,
"Power Macro-Models for High-Level Power Estimation",
in *Low Power Electronics Design*,
C. Piguet Editor, CRC Press, Boca Raton, Florida, 2004.
4. K. Patel, E. Macii, *M. Poncino*,
"Energy-Efficient Shared-Memory Architectures for Multi-Processor Systems-on-Chip,"
in *Ultra Low-Power Electronics and Design*,
Kluwer Academic Publishers, Boston, 2003.
5. L. Benini, *M. Poncino*,
Ambient Intelligence: A Computational Perspective,
in *Ambient Intelligence: Impact on Embedded-system Design*,
Kluwer Academic Publishers, Boston, 2003.

Articoli su riviste internazionali

1. A. Lioy, *M. Poncino*,
"A Study of the Resetability of Synchronous Sequential Circuits,"
Microprocessing and Microprogramming,
Vol 38, pp. 395–402, November 1993.
2. D. Abvisio, S. Cianchini, E. Macii and *M. Poncino*,
"A Sequential Circuit Simulator Based on Hybrid Cellular Automata",
Systems Analysis, Modelling and Simulation,
Vol 16, pp. 245–253, 1994.
3. D. Abvisio, S. Cianchini, E. Macii, *M. Poncino*,
"Modeling Sequential Circuits with Cellular Automata",
International Journal of Systems Science,
Vol 26, No. 7, pp. 1415–1428, July 1995.
4. E. Macii, *M. Poncino*,
The Impact of Cell Library Characteristics on Area, Speed, and Power Consumption of CMOS Circuits,"
International Journal on Electronics,
Vol 78, No. 2, pp. 395–407, 1995.
5. E. Macii, *M. Poncino*,
"Symbolic Reation and Manipulation of Large Neural Networks",
ISCA International Journal on Computers and their Appplications,
Vol 11, No. 2, pp. 104–111, August 1995.
6. E. Macii, *M. Poncino*,
"Using Connectivity and Spectral Methods to Characterize the Structure of Sequential Logic Circuits,"
Microprocessing and Microprogramming,
Vol 41(1995), pp. 487–500.
7. E. Macii and *M. Poncino*,
"Using Symbolic Rademacher-Walsh Spectral Transforms to Evaluate the Agreement
Between Boolean Functions",
IEE Proceedings – Computers and Digital Techniques,
Vol 143, No. 1, pp. 64–68, January 1996.
8. E. Macii, *M. Poncino*,
"Estimating Power Consumption of CMOS Circuits Modeled as Symbolic Neural Networks",
IEE Proceedings – Computers and Digital Techniques,
Vol 143, No. 5, pp. 331–336, September 1996.
9. H. Cho, G. D. Hachtel, E. Macii, *M. Poncino*, and F. Somenzi,
"Automatic State Space Decomposition for Approximate FSM Traversal Based on
Circuit Structural Analysis,"
IEEE Transactions on CAD,
Vol 15, No. 12, pp. 1451–1464, December 1996.
10. E. Macii, *M. Poncino*,
" An Exact Algorithm for Computing the Entropy of a Logic Circuit,"
ISCA: International Journal on Computers and their Applications,
Vol 4, No. 2, pp. 49-55, 1997.
11. E. Macii, *M. Poncino*,
"An Application of Hopfield Neural Networks to Symbolic Power Analysis of VLSI Digital Circuits,"
International Journal of Engineering Science,

Vol 35, No. 8, pp. 783-792, 1997.
12. E. Macii, *M. Poncino*,
"Predicting the Complexity of Large Combinational Circuits Through Symbolic Spectral Analysis of their Functional Specifications",
IEE Proceedings – Computers and Digital Techniques,
Vol 144, No. 5, pp. 343-347, 1997.
13. E. Macii, *M. Poncino*,
"Cellular Automata Models for Reliability Analysis of Systems on Silicon,"
IEEE Transactions on Reliability,
Vol 46, No. 2, June 1997, pp. 173–183.
14. F. Ferrandi, F. Fummi, E. Macii, *M. Poncino*, D. Sciuto,
"Testing Core-Based Digital Systems: A Symbolic Methodology",
IEEE Design & Test, Vol 14, No. 4, pp. 69–77, October/December 1997.
15. A. H. Evans, E. Macii, *M. Poncino*,
"Re-Synthesis for Testability of Redundant Combinational Circuits",
Microcomputer Applications,
Vol 17, No. 1, pp. 8-11, 1998.
16. E. Macii, *M. Poncino*,
"Automatic Synthesis of Easily Scalable Architecture for Bus Arbiters with Dynamic Priority Assignment Strategies,"
Computers and Electrical Engineering: An Internation Journal, Vol 24 (1998), pp. 223–228.
17. L. Benini, G. De Micheli, E. Macii, *M. Poncino*,
"Telescopic Units: A New Paradigm for Performance Optimization of VLSI Designs"
IEEE Transactions on CAD, Vol 17, No. 3, pp. 220–232, March 1998.
18. L. Benini, G. De Micheli, E. Macii, *M. Poncino*, S. Quer,
"Power Optimization of Core-Based Systems by Address Bus Encoding,"
IEEE Transactions on VLSI Systems, Vol 6, No. 4, pp. 554-562, Dicembre 1998.
19. L. Benini, G. De Micheli, A. Macii, E. Macii, *M. Poncino*,
"A Methodology for the Automatic Selection of Instruction Op-Codes of Low-Power Core Processors,"
IEE Proceedings – Computer & Digital Techniques, Vol 146, No. 4, July 1999, pp. 173–178.
20. L. Benini, G. De Micheli, A. Lioy, E. Macii, G. Odasso, *M. Poncino*,
"Automatic Synthesis of Large Telescopic Units Based on Near-Minimum Timed Supersetting,"
IEEE Transactions on Computers, Vol 48, No. 8 , pp. 769–779, August 1999.
21. M. Baldi, E. Macii, *M. Poncino*,
"Probabilistic Analysis and Verification of Communication Protocols Based on Symbolic FSM Manipulation"
IEE Proceedings – Computer & Digital Techniques, Vol 146, No. 5, September 1999, pp. 221–226.
22. L. Benini, G. De Micheli, E. Macii, *M. Poncino*, R. Scarsi,
"Symbolic Synthesis of Clock-Gating Logic for Power Optimization of Synchrounous Controllers,"
ACM Transactions on Design Automation of Electronic Systems, Vol 4, No. 4, October 1999, pp. 351–375.
23. L. Benini, G. De Micheli, E. Macii, *M. Poncino*, R. Scarsi,
"A Multi-Level Scheme for Fast Power Simulation of Realistic Input Streams,"
IEEE Transactions on CAD, Vol 19, No. 3, April 2000, pp. 459–472.
24. L. Benini, A. Macii, E. Macii, *M. Poncino*,
"Increasing Energy Efficiency of Embedded Systems by Application-Specific Memory Hierarchy Generation,"
IEEE Design and Test, Vol 17, No. 2, April/June 2000, pp. 74–85.
25. L. Benini, G. De Micheli, A. Macii, E. Macii, *M. Poncino*, R. Scarsi,
"Glitch Power Minization by Selective Gate Freezing",
IEEE Transactions on VLSI Systems, Vol 8, No. 3, June 2000, pp. 287–298.
26. F. Ferrandi, F. Fummi, E. Macii, *M. Poncino*, D. Sciuto,
"Symbolic Optimization of FSM Networks Based on Redundancy Identification and Removal",
IEEE Transactions on CAD, Vol 19, No. 7, July 2000, pp. 760–772.
27. L. Benini, A. Macii, E. Macii, *M. Poncino*, R. Scarsi,
Architectures and Synthesis Algorithms for Power-Efficient Bus Interfaces",
IEEE Transactions on CAD, Vol 19, No. 9, September 2000, pp. 969–980.
28. A. Macii, E. Macii, *M. Poncino*, R. Scarsi,
"Stream Synthesis for Efficient Power Simulation Based on Spectral Transforms,"
IEEE Transactions on VLSI Systems, Vol 9, No. 1, June 2001, pp 417–426.
29. L. Benini, G. De Micheli, A. Lioy, E. Macii, G. Odasso, M. Poncino,
"Synthesis of Power-Managed Sequential Components Based on Computational kernel Extraction,"
IEEE Transactions on CAD, Vol 9, No. 9, September 2001, pp .1118–1131.
30. L. Benini, G. Castelli, A. Macii, E. Macii, M. Poncino, R. Scarsi,
"Discrete-Time Battery Models for System-Level Low-Power Design",
IEEE Transactions on Very Large Scale Integration (VLSI) Systems,

Vol 9, No. 5, pp. 630-640, October 2001.
31. A. Bogliolo, R. Corgnati, E. Macii, M. Poncino,
"Parameterized RTL Power Models for Soft Macros",
IEEE Transactions on Very Large Scale Integration (VLSI) Systems,
Vol 9, No. 6, pp. 880-887, December 2001.
32. A. Macii, E. Macii, M. Poncino,
"Current-Controlled Battery Management Policies for Lifetime Extension of Portable Systems",
ST Journal of System Research,
Vol 3, No. 1, pp. 92-99, April 2002.
33. L. Benini, L. Macchiarulo, A. Macii, E. Macii, M. Poncino,
"Layout-Driven Memory Synthesis for Embedded Systems-on-Chip,"
IEEE Transactions on VLSI Systems,
Vol 10, No. 2, pp. 96-105, April 2002.
34. M. Baldi, A. Macii, E. Macii, M. Poncino,
"VHDL Simulation: A Flexible Approach to Protocol Verification and Performance Analysis",
Systems Analysis, Modelling and Simulation,
Vol 42, No. 6, pp. 925-938, June 2002.
35. L. Benini, A. Macii, E. Macii, M. Poncino,
"Minimizing Memory Access Energy in Embedded Systems by Selective Instruction Compression",
IEEE Transactions on Very Large Scale Integration (VLSI) Systems,
Vol 10, No. 5, pp. 521-531, October 2002.
36. L. Benini, A. Macii, M. Poncino,
"Energy-Aware Design of Embedded Memories: A Survey of Technologies, Architectures and Optimization Techniques",
ACM Transactions on Embedded Computing Systems,
Vol 2, No. 1, pp. 5–32, February 2003.
37. L. Benini, D. Bertozzi, D. Bruni, N. Drago, F. Fummi, M. Poncino,
"SystemC Co-Simulation and Emulation of Multi-Processor Systems-on-Chip,"
IEEE Computer,
Vol 36, No. 4, pp. 53–59, April 2003
38. L. Benini, D. Bruni, A. Macii, E. Macii, M. Poncino,
"Extending Lifetime of Multi-Battery Mobile Systems by Discharge Current Steering",
IEEE Transactions on Computers,
Vol 52, No. 8, pp.985-995, August 2003.
39. L. Benini, G. Castelli, A. Macii, E. Macii, M. Poncino, R. Scarsi,
"Scheduling Battery Usage in Mobile Systems",
IEEE Transactions on Very Large Scale Integration (VLSI) Systems,
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